(iv) A bipolar transistor uses a current into its base to control a large current between collector and emitter whereas a *JFET* uses *voltage* on the 'gate' (= base) terminal to control the current between drain (= collector) and source (= emitter). Thus a bipolar transistor gain is characterised by current gain whereas the *JFET* gain is characterised as a transconductance *i.e.*, the ratio of change in output current (drain current) to the input (gate) voltage.

(v) In *JFET*, there are no junctions as in an ordinary transistor. The conduction is through an *n*- type or *p*-type semi-conductor material. For this reason, noise level in *JFET* is very small.

21.7. JFET as an Amplifier

Fig. 21.6 shows *JFET* amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of *JFET*, the gate must be negative *w.r.t.* source *i.e.*, input circuit should always be reverse biased. This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit. In the present case, we are providing biasing by the battery V_{GG}.

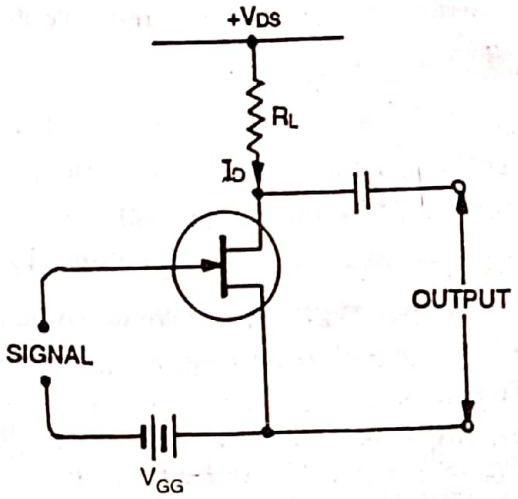

Fig. 21.6

A small change in the reverse bias on the gate produces a large change in drain current. This fact makes *JFET* capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current. During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases. The result is the small change in voltage at the gate produces a large change in drain current. These large variations in drain current produce large output across the load R_L. In this way, *JFET* acts as an amplifier.

21.8. Output Characteristics of JFET

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a *JFET* at constant gate-source voltage (V_{GS}) is known as *Output characteristics of JFET*. Fig. 21.7 shows the circuit

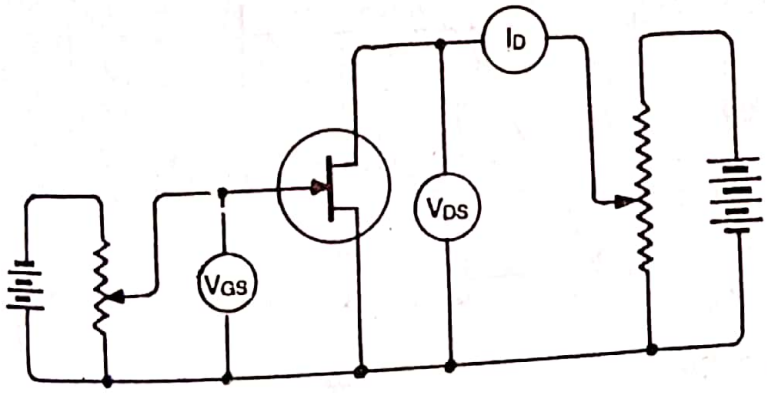

Fig. 21.7.

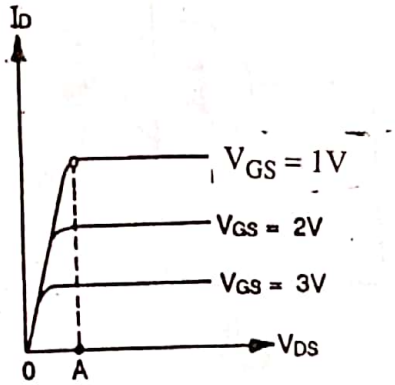

Fig. 21.8.

for determining the output characteristics of *JFET*. Keeping V_{GS} fixed at some value, say 1V, the drain-source voltage is changed in steps. Corresponding to each value of V_{DS}, the drain current

I_D is noted. A plot of these values gives the output characteristic of *JFET* at $V_{GS} = 1V$. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. 21.8 shows a family of output characteristics.

The following points may be noted from the characteristics :

(i) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant. The drain-source voltage above which drain current becomes constant is known as *pinch off voltage*. Thus in Fig. 21.8, *OA* is the *pinch off voltage*.

(ii) After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other. The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch off voltage. Consequently, drain current remains constant.

(iii) The characteristics resemble that of a pentode valve.

21.9. Important Terms

In the analysis of a *JFET* circuit, the following important terms are often used :

1. Shorted-gate drain current (I_{DSS})
2. Pinch off voltage (V_P)
3. Gate-source cut off voltage [$V_{GS(off)}$]

1. Shorted-gate drain current (I_{DSS}). *It is the drain current with source short-circuited to gate (i.e. $V_{DS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage.* It is sometimes called *zero-bias current.*

Fig 21.9 shows the *JFET* circuit with $V_{GS} = 0$ *i.e.,* source shorted-circuited to gate. This is normally called shorted-gate condition. Fig. 21.10 shows the graph between I_D and V_{DS} for the shorted gate condition. The drain current rises rapidly at first and then levels off at pinch off voltage V_P. The drain current has now reached the maximum value I_{DSS}. When V_{DS} is increased beyond V_P, the depletion layers expand at the top of the channel. The channel now acts as a current limiter and *holds drain current constant at I_{DSS}.

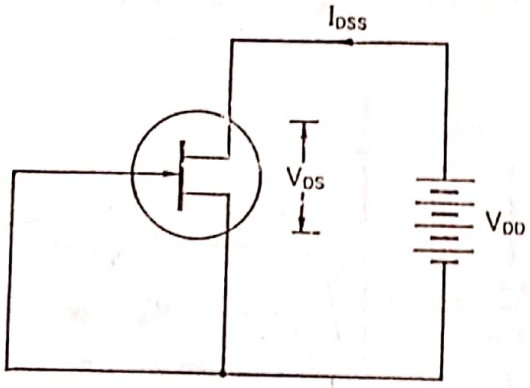

Fig. 21.9

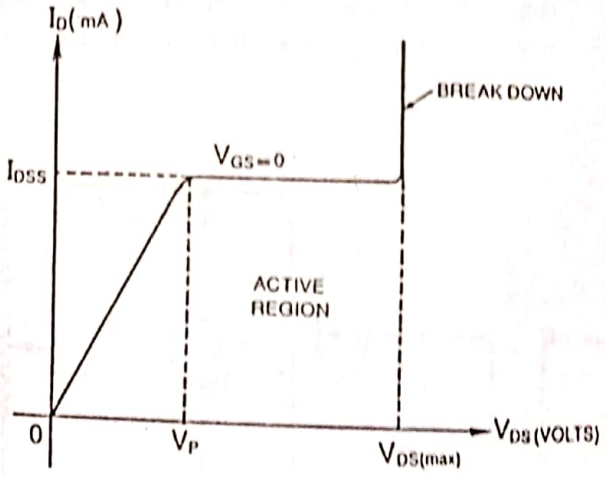

Fig. 21.10

* When drain voltage equals V_P, the channel becomes narrow and the depletion layers almost touch each other. The channel now acts as a current limiter and holds drain current at a constant value of I_{DSS}.

The following points may be noted carefully :

(i) Since I_{DSS} is measured under shorted gate conditions, it is the maximum drain current that you can get with normal operation of *JFET*.

(*ii*) There is a maximum drain voltage [$V_{DS(max)}$] that can be applied to a *JFET*. If the drain voltage exceeds $V_{DS(max)}$, *JFET* would breakdown as shown in Fig. 21.10.

(*iii*) The region between V_P and $V_{DS(max)}$ (breakdown voltage) is called *constant-current region* or active region. As long as V_{DS} is kept within this range, I_D will remain constant for a constant value of V_{GS}. In other words, in the active region, *JFET* behaves as a constant-current device. For proper working of *JFET*, it must be operated in the active region.

2. Pinch off Voltage (*VP*). *It is the minimum drain-source voltage at which the drain current essentially becomes constant.*

Figure 21.11 shows the drain curves of a *JFET*. Note that pinch off voltage is V_P. The highest curve is for $V_{GS} = 0$, the shorted-gate condition. For values of V_{DS} greater than V_P, the drain current is almost constant. It is because when V_{DS} equals V_P, the channel is effectively closed and does not allow further increase in drain current. It may be noted that for proper function of *JFET*, it is always operated for $V_{DS} > V_P$. However, V_{DS} should not exceed $V_{DS(max)}$ otherwise *JFET* may breakdown.

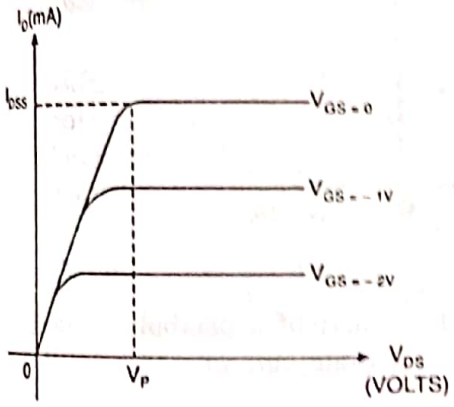

Fig 21.11

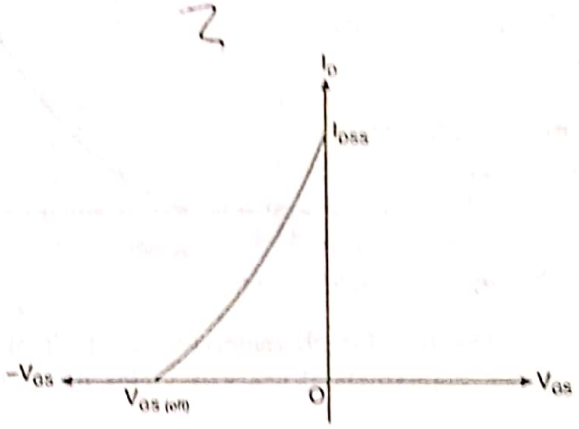

Fig 21.12

3. Gate-source cut off voltage $V_{GS(off)}$. *It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.*

The idea of gate-source cut off voltage can be easily understood if we refer to the transfer characteristic of a *JFET* shown in Fig. 21.12. As the reverse gate-source voltage is increased, the cross-sectional area of the channel decreases. This in turn decreases the drain current. At some reverse gate-source voltage, the depletion layers extend completely across the channel. In this condition, the channel is cut off and the drain current reduces to zero. The gate voltage at which the channel is cut off (*i.e.* channel becomes non-conducting) is called gate-source cut off voltage $V_{GS(off)}$.

Notes. (*i*) It is interesting to note that $V_{GS\,(off)}$ will always have the same magnitude value as V_p. For example if $V_p = 6V$, than $V_{GS\,(off)} = -6V$. Since these two values are always equal and opposite, only one is listed on the specification sheet for a given *JFET*.

(*ii*) There is a distinct difference between V_p and $V_{GS\,(off)}$. Note that V_P is the value of V_{DS} that causes the *JFET* to become a constant current device. It is measured at $V_{GS} = 0V$ and will have a constant drain current $= I_{DSS}$. However, $V_{GS\,(off)}$ is the value of V_{GS} that causes I_D to drop to nearly zero.

21.10. Expression for Drain Current (I_D)

The relation between I_{DSS} and V_P is shown in Fig. 21.13. We note that gate-source cut off voltage [*i.e.* $V_{GS(off)}$] on the transfer characteristic is equal to pinch off voltage V_P on the drain characteristic *i.e.*

$$V_P = \left| V_{GS\,(off)} \right|$$

For example, if a *JFET* has $V_{GS} = -4V$, then $V_P = 4V$.

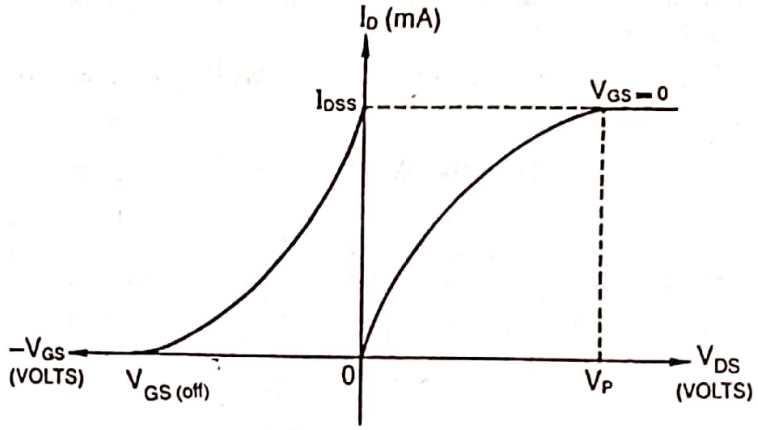

Fig. 21.13

The transfer characteristic of JFET shown in Fig. 21.13 is part of a parabola. A rather complex mathematical analysis yields the following expression for drain current :

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

where I_D = drain current at given V_{GS}

I_{DSS} = shorted–gate drain current

V_{GS} = gate–source voltage

$V_{GS\,(off)}$ = gate–source cut off voltage

Example 21.1. *Fig. 21.14 shows the transfer characteristic of a JFET. Write the equation for drain current.*

Solution

Referring to the transfer characteristic in Fig. 21.14, we have,

V_{DSS} = 12mA

$V_{GS\,(off)} = -5V$